

CLAIMS:

- 1 1. A time-of-flight (TOF) system integrated onto a single chip for measuring
2 precise time intervals, said system comprising:
3 a first constant fraction discriminator for receiving an analog start signal input
4 and providing a digital output representative of the start signal;
5 a second constant fraction discriminator for receiving an analog stop signal
6 input and providing a digital output representative of the stop signal;
7 a logic circuit coupled with the first and second constant fraction
8 discriminators for determining a Δt time interval between the start and stop signals;
9 and
10 a time-to-digital converter (TDC) receiving as input the Δt time interval
11 between the start and stop signals, said time-to-digital converter for digitizing the Δt
12 time interval with reference to an off-chip precise reference clock.
- 1 2. The system of claim 1 further comprising valid event logic coupled with the
2 time-to-digital converter, the valid event logic for rejecting invalid events.
- 1 3. The system of claim 1 further comprising a phase locked loop coupled with
2 the time-to-digital converter, the phase locked loop for providing a time reference to
3 the off-chip reference clock and to compensate for temperature and power supply
4 variations.

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1 4. The system of claim 1 further comprising adder logic coupled with the time-to-
2 digital converter, the adder logic for correcting for timing offset.

1 5. The system of claim 1 wherein the output of the time-of-flight chip is an 11-bit
2 linear word.

1 6. The system of claim 1 wherein the output of the time-of-flight chip is an 8-bit
2 compressed word.

1 7. The system of claim 1 wherein original digital start and stop signals can be
2 directly input to the time-to-digital converter bypassing the constant fraction
3 discriminators.

1 8. The system of claim 1 wherein each constant fraction discriminator
2 comprises:

3 an arming comparator having built-in hysteresis for avoiding multi-firing around
4 a threshold), said arming comparator for receiving a positive input pulse wherein the
5 arming comparator fires when the positive input pulse crosses a threshold;

6 a zero crossing comparator for receiving a delayed version of the positive
7 input pulse and an attenuated version of the positive input pulse wherein the zero
8 crossing comparator fires at a constant fraction of the positive input pulse; and

9 a logical AND gate coupled with a one-shot for receiving the output of the
10 arming comparator and the zero crossing comparator, the AND gate and one-shot

11 providing a digital output for the constant fraction discriminator.

1 9. The system of claim 8 wherein each constant fraction discriminator further
2 comprises an on-chip analog delay line.

1 10. The system of claim 1 wherein the time-to-digital converter comprises:
2 a time difference generating logic component for determining a start-stop time
3 difference defined by the rising edges of two positive going signals ;
4 a time reference generating logic component for applying a train of negative
5 going pulses from the reference clock to a calibration delay locked loop DLL;
6 a core of time-to-digital converter cells for receiving a valid negative going
7 pulse of duration equal to the start-stop time difference wherein each cell
8 truncates the valid negative going pulse by a fixed time; and
9 a position decoding component for determining the cell location where the
10 valid negative going pulse disappeared.

1 11. The system of claim 10 wherein each time-to-digital converter cell is
2 comprised of:
3 a current starving inverter; and
4 a standard inverter coupled with the current starving inverter,
5 such that a negative pulse of duration T entering a time-to-digital
6 converter cell yields a negative output pulse with a controllable reduced
7 duration.